# Research on VHDL in France, Italy and Switzerland

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**Abstract**

This presentation is an overview of the research on and around VHDL in France, Italy and French speaking Switzerland. The teams covered by this survey are well known in Europe, for their participation in the VHDL User's Groups, and for their publications. The period covered is 1991-1995, although some groups have started their VHDL activities several years before.

## 1. Introduction

European research has largely contributed to the state of the art concepts in Hardware Description Languages, and their associated CAD software. Because so many HDL's had been developed in Europe, probably more than in other continents has VHDL been rapidly adopted by academic as well as industry, for its status as a standard. This paper surveys the research, primarily academic, on and around VHDL in three neighbour countries: France, Italy and the French speaking part of Switzerland. Other papers in the same session cover other countries and tongues.

A questionnaire has been sent around in November and December 1995; the informations contained in this paper are largely based on the answers received, and can therefore be considered current at the time of publication. Although not exhaustive (groups with a recent VHDL involvement might have been forgotten, and some questionnaires did not come back), this survey should give the reader an idea about the variety and the vitality of VHDL-based activities in the geographical area covered.

The paper is organized as follows: first a table gives a global view on the research groups, their topic areas and their main achievements in direct relation to VHDL. As a matter of fact, the main scientific contribution of some groups is independent of VHDL, in which case only their VHDL-related results are listed in the table. Then the overall theoretical and practical achievements of each group are analyzed in more detail, and a contact person and list of references is provided.

Countries are presented in alphabetical order. In each country, research laboratories in the same city are next to each other. Otherwise, the order in which the institutions are listed in each country is irrelevant.

### 2. IRISA, Rennes, France [1-6]

The EPATR (in English: Programming Environment for Real-Time Applications) research group is large of about 20 persons, and headed by Paul Le Guernic (e-mail: Paul.LeGuernic@irisa.fr). Their primary interest is the development of a complete set of tools for the development of real-time systems, including specification, simulation, formal verification and code generation. An important aspect in their current research activities is hardware/software codesign. They are famous for the definition of the SIGNAL synchronous design language for the specification of real-time applications. In this context, their interest in VHDL, which started in 1992, aims primarily at linking to hardware development (simulation and synthesis) tools and secondly at formally verifying hardware descriptions using SIGNAL.

With respect to VHDL, the following results have been obtained:

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| Affiliation | Research Area | Achievements | Still active in VHDL |
|---|---|---|---|
| IRISA, Rennes France | High level synthesis<br>Formal semantics for VHDL | Prototype Signal to VHDL Translator | Yes |
| TIMA, Grenoble France | High level synthesis | AMICAL High-level synthesis tool (distributed) | Yes |
| ARTEMIS, Grenoble in coop. with Univ. de Provence, Marseille, France | Formal semantics for VHDL (denotational, FSM,LTS)<br>Formal verification from VHDL | PREVAIL formal verification environment (distributed) | Yes |
| MASI, Univ. Paris 6 France | High level synthesis<br>Formal semantics for VHDL (Petri Nets)<br>Formal verification from VHDL | ALLIANCE CAD system ( distributed)<br>Prototype Model Checker | Yes |
| Univ. Evry, France | Formal semantics for VHDL<br>Object-oriented extension | SDEV: Syntactic Driven Editor for VHDL (distributed) | Yes |
| CERT, Toulouse France | High level synthesis<br>Formal semantics for VHDL | L2V: Lustre to VHDL Translator (available) | No |
| LAAS, Toulouse, France | Fault injection,<br>Fault simulation | MEFISTO: Fault injection and simulation | Yes |
| Phase Lab.<br>Univ. Strasbourg France | Distributed Simulation of VHDL and VHDL-A on a network of workstations | Prototype under development | Yes |
| Politecnico di Milano, Italy | Logic and high level synthesis<br>Test and testability | Prototype for testability analysis and test pattern generation | Yes |
| Univ. La Sapienza, Roma, in coop. with Univ. di Firenze, Italy | Formal semantics for VHDL (Process algebra)<br>Formal verification | Theoretical results | Yes<br>in Firenze |
| Politecnico di Torino Italy in coop. with EDF-research, France | High level specification (VOVHDL)<br>Formal semantics (LTS)<br>Formal verification | VOVHDL to ASA+ translator | Yes |
| Ecole Polytechnique Fédérale de Lausanne, Switzerland | Analog VHDL | Involvement in A-VHDL WG | Yes |

**Table: Research Groups reviewed, and their VHDL-related achievements**

1) Definition of a framework for the formal verification of VHDL descriptions using the SIGNAL language [1-3], based on the semantic definition of a VHDL subset in SIGNAL, the construction of an interface between SIGNAL and VHDL, and the embedding of the VHDL simulation model under SIGNAL.

2) Development of a prototype code generator from SIGNAL (with restrictions) to VHDL, in order to use resulting VHDL models as input to synthesis tools; possible target architectures have been defined, and hybrid (synchronous/asynchronous) circuit descriptions are accepted [4-6]. This tool is still experimental and thus not available in the current distribution of the SIGNAL environment.

Present research activities are strongly involved with VHDL, and include: extending the mapping of SIGNAL to VHDL to be able to translate all SIGNAL programs into VHDL, improving the quality of the VHDL code generated, the generation of structural VHDL from a SIGNAL graphical description, and the generation of VHDL models for the hardware partition of a hybrid systems as well as the interface between the software and hardware of the system.

## 3. TIM-A Laboratory, I.N.P.G. and U.J.F., Grenoble, France [7-14]

The "System Level Synthesis" reseach group of TIMA gathers fifteen persons under the direction of Ahmed Jerraya. They started their research on High Level Synthesis from VHDL in 1990, and more recently got involved into C-VHDL co-simulation methods and tools.

The group is well known for the development of the AMICAL system[7-12], a High Level Synthesis tool with design re-use, that takes behavioral VHDL descriptions, and produces a RTL level synthesized system, according to user defined parameters. The user interface has received particular attention, with simultaneous display of a graphic and a VHDL representation of the resulting system, that the designer may interactively modify to explore the design space. The AMICAL system is well documented, largely distributed, and available by anonymous ftp.

Another prototype, called VCI, is also under development. VCI generates an interface for co-simulation of VHDL and C models. The tool is not yet available.

The group current research areas are Design Re-use within Behavioral Synthesis[14], and C-VHDL Co-simulation [13]. More informations may be obtained by e-mail: Ahmed-Amine.Jerraya@imag.fr.

## 4. ARTEMIS Laboratory, I.N.P.G. and U.J.F., Grenoble, France [15-28]

The "Modeling and Verification of Digital Systems" research group headed by Dominique Borrione gathers eight persons, PhD's included. Due to the restructuring of the Computer Science research laboratories in Grenoble, this group has joined the TIM-A Laboratory in January 1996. The senior researchers of this group have worked in the field of CAD of digital and electronic circuits for over 20 years, and have a long experience in the design of Computer Hardware Description Languages (CHDL's), simulators, and integration of various CAD tools. They have been involved in VHDL standardization from its start, and in several VHDL working groups (Analog Extension, Synthesis WG, Shared Variable WG). The main research areas are: HDL design, Formal Semantics, Formal Verification, Mixed-Mode Simulation.

Most of the research has been performed in close cooperation with several European academic teams, within the ESPRIT CHARME project, and with various French industrial partners, notably through French national projects, and the JESSI AC3 project. The main theoretical and practical results obtained are:

1) The formal definition of a synchronous VHDL subset, called P-VHDL, in terms of finite state machines (FSM's). A symbolic model checker SMOCK has been developped for P-VHDL, where the properties to be checked are expressed in a branching time temporal logic that extends CTL to include also modalities looking to the past[19-21].
2) A denotational semantic definition for P-VHDL [17, 24, 25].
3) Proposals for the Analog extension of VHDL, and the implementation of a mixed mode simulation kernel, in cooperation with CNET and Anacad [22, 23].
4) The elaboration of a semantic model in terms of labelled transition systems, for the inter-process communications and synchronizations in VOVHDL and in VHDL'93, in cooperation with EDF Research (Les Renardières, France) and Politecnico di Torino (Italy)[15, ].
5) The formal validation of a significant portion of the recently approved Numeric_Bit and Numeric_Std standard synthesis packages, using the Boyer-Moore NQTHM theorem prover (distributed by CLI, Texas, USA) [18].
6) The development of the PREVAIL™ proof environment prototype[27, 28]. This system is built around a kernel internal Proof-oriented Intermediat Form (PIF), and an interactive user-interface. Translators have been written from P-VHDL to PIF, and from PIF to the input of various tools: the FSM equivalence checker LOVERT of Frankfurt University (Germany), SMOCK, and the group's new prototype diagnostic and automatic correction software for combinational and sequential circuits. PREVAIL is available, distributed to partner Universities, and minimal on-line documentation exists. E-mail contact: Hakim.Bouamama@imag.fr or Dominique.Borrione@imag.fr

Current research works include:

- the development of a library of functions and theorems that model VHDL primitives in the logic of Boyer-Moore, and of an automatic translator from PIF to the NQTHM input language;
- the extension of P-VHDL with some of the new primitive concepts added in VHDL'93.

## 5. Université de Provence, Marseille, France [27-32]

The "Formal Verification" group of Marseille Computer Science Laboratory gathers seven persons on the theme of formal verification of high level systems description, with an emphasis on the use of general purpose theorem provers (based on first as well as higher-level logic). Among them, two persons are directly working on formal semantics for VHDL and formal verification from VHDL descriptions since 1990, in cooperation with other European academic teams, within the ESPRIT CHARME project and French national projects; and recently a study was started on the evaluation of VHDL for the specification of distributed architectures and reactive systems.

The following achievements are related to VHDL:

1) the development of proofs for various types of VHDL generic descriptions, using the NQTHM theorem prover of Boyer and Moore: structural synchronous sequential circuits, parallel multipliers, behavioral descriptions with functions and processes[29, 30].
2) participation to the development of the PREVAIL system, notably concerning the translation from VHDL to NQTHM, in cooperation with ARTEMIS [27, 28].

In relation with VHDL, current topics of investigation are:

- the definition of a functional semantics for VHDL in the logic of Boyer and Moore
- a comparative study of VHDL with more formal languages such as LOTOS or UNITY, for the specification of distributed architectures and of reactive systems[31, 32].

## 6. Paris 6 University, France [33-39]

Laboratoire MASI at Université Pierre et Marie Curie (Paris 6) has a long standing experience in the development of CAD tools that are widely distributed among French universities for teaching and research purposes. Two teams have a strong VHDL involvement, and are reviewed in this paper.

**6.1 The "Computer Architecture" research group**, headed by Alain Greiner (e-mail: Alain.Greiner@masi.ibp.fr) started working with VHDL in 1989. Their primary interest is the development of CAD for VLSI and integrated systems, from RTL specifications down to the silicon.

They have defined a small subset of VHDL for simulation, logic and finite state machine synthesis, and formal proof. This subset includes only the parallel statements of VHDL: data-flow style and structural netlist description.

The group has developped the ALLIANCE system [33-35], which is a complete CAD system for the specification, design and validation of VLSI circuits described in the VHDL subset. ALLIANCE includes the following tools:

- ASIMUT: RTL VHDL simulation tool
- LOGIC: Boolean optimizer and logic synthesis (mapping) tool
- PROOF: Formal prover of combinatorial logic (the registers must be identical in both descriptions to be proved identical)
- ALLIGATOR: Logic synthesis for Xilinx FPGAs
- DESB: Gate level extractor that generates VHDL equations from a netlist of transistors

ALLIANCE is largely distributed in French and European Universities, and routinely used in teaching. Its documentation includes a user manual, tutorials and theses. It is available by ftp at: //ftp.ibp.fr/ibp/softs/masi/alliance

Current research in relation with VHDL includes power estimation and formal proof of sequential circuits. The present VHDL subset is also being extended to sequential statements to make it roughly Synopsys compatible.

**6.2 The research group titled "Numeric algorithms and parallelism"**, headed by Michel Minoux (e-mail: Michel.Minoux@masi.ibp.fr), is concentrating on Formal Semantics for VHDL and Formal verification from VHDL since the end of 1992. They have defined a formal semantics of a subset of VHDL in terms of Petri Nets, and developed two prototype tools:

1) VPN (VHDL towards Petri Net) performs the construction of a symbolic representation of VHDL behaviors in terms of Petri Nets[36, 38], on which
2) VMC (VHDL Model Checker) [37] applies symbolic state space traversal algorithms to verify CTL properties of VHDL programs. The tool has been demonstrated, but is not available, and is currently being extended to cover a larger VHDL subset.

Present research areas include the automatic verification of the equivalence of two VHDL models and synthesis of VHDL behavioral descriptions[39].

## 7. University of Evry, France [40-42]

The research group "Specifications of Architectures" of Laboratoire Mathematiques/Informatique at Université d'Evry Val d'Essonne is headed by Michel Israel; it gathers three academics and five PhD's. Their work on VHDL started in 1989, and is still going on. The main topic interests are: High Level Synthesis, Object Oriented extensions to VHDL, Formal Semantics for VHDL, Formal Verification from VHDL, Test and Reliability. The group has been involved in the VHDL'93 standardization, and in the OOVHDL WG chaired by Doug DUNLOP.

They have developed SDEV [40-42]: A Syntactic Driven Editor for VHDL, which allows the user to tailor his own VHDL subset and check if VHDL programs are syntactically correct, based upon Synopsys subset or other VHDL subsets. The software is available and already distributed; documentation is not yet written. The contact person is Ms Judith Benzakki, e-mail: benzakki@lami.univ-evry.fr.

Current work focuses on:

- extensions (Object Oriented) of VHDL to add more abstraction for reuse in High Level Synthesis
- VHDL semantics using the formalism called ETOILE (algebraic specifications)

## 8. Centre d'Etudes et de Recherches de Toulouse, France

A small group at CERT participated in the "ASAR" project, in cooperation with the above mentioned team from Evry. Their involvement with VHDL started in 1991, and concerned mainly High level synthesis and Formal Semantics for VHDL. This group is no longer active on VHDL.

Within the "ASAR" project, they developed the "L2V" prototype translator from LUSTRE (a stream-based synchronous language) to VHDL. L2V is written in CAML 6.0, and is available upon request. Documentation is in French. The contact person is Michel Lemaitre, e-mail: Michel.Lemaitre@cert.fr.

## 9. Laboratoire d'Automatique et d'Analyse de Systèmes, Toulouse, France [43-48]

The "Dependable Computing and Fault Tolerance" research group headed by Jean-Claude Laprie at LAAS is composed of 10 permanent researchers and 11 PhD students. Within that group, three persons are working on VHDL models. In order to validate fault tolerance mechanisms early in the design of fault tolerant systems, they are focusing on the application of fault injection in simulation models so that their validation can be readily integrated in the development process. Activities on fault injection in VHDL models started in 1991, and have been performed partly in cooperation with Chalmers University (Goteborg, Sweden) in the framework of the "Predictably Dependable Computing Systems" ESPRIT project. Current topics of interest include fault models, reliability, and extensions to VHDL to ease the application of fault injection in VHDL models[44].

The main VHDL-related achievement of this group is the prototype tool called MEFISTO (Multi-level Error/Fault Injection Simulation TOol) that supports the application of two fault injection mechanisms specifically defined for VHDL models[43-47]:

1) insertion of generic constructs (called "saboteurs") into the VHDL code to inject faults at the level of signals,
2) carry out "mutations" of the VHDL code.

The software has been demonstrated at international meetings, but is not yet available. The contact person is Jean Arlat, e-mail: arlat@laas.fr.

Current research focuses on guiding the derivation of test patterns to specify fault injection experiments aimed at testing fault tolerance mechanisms modeled by means of a simulation language, VHDL being the major target language.

## 10. Strasbourg University, France [49]

The AMCAD (Advanced Methods for CAD) group at PHASE (Physics and Application of Semiconductors) Laboratory is composed of two academics and eight students. Their involvement on VHDL started in 1991, with actual implementation work since 1994, in cooperation with LIS in Sevenans and MASI in Paris. Their primary research area is Distributed Simulation of VHDL and its Analog extension on a network of workstations. The Web page for the group is http://www.sneezy.u-strasbg.fr:80/~yann/macao.html

They have developed an algorithm to extract the parallelism in VHDL models, which performs on-the-fly computation during a sequential simulation. A distributed VHDL simulator is being implemented, and should be available by the end of 1996. The tools is decomposed into the following modules:

- VSEQ: reference sequential simulator
- VMAC: macroparallelization (communicating sequential simulators, built on an extension of the SPEEDES algorithm)
- VMIC: microparallelization (where one or more VHDL process is implemented by one UNIX process)
- F_SAV: environment that integrates the various modules, for parameter fixing and results analysis.

Current research aims at developping a distributed simulator for the Analog extension of VHDL, with particular focus on the placement and synchronization problems.
In addition, the group manages a VHDL archive of testbenches which can be accessed by anonymous ftp at: erm1.u-strasbg.fr.

## 11. Politecnico di Milano, Milano, Italy [50-58]

Within the "Hardware Architectures" group of the Electrical Engineering and Information Science Department, a research team of eight academics plus students forms the "Design Methodologies" group. They started working

with VHDL in 1991, and their primary interest areas are Logic Synthesis, High Level Synthesis, Test and Testability, and Fault models.

Among the main achievements of this group, we can mention:

1) Definition of a methodology for synthesis, for testability and test pattern generation of FSM based circuits, starting from RTL-level VHDL [50-52]. Software has been developed for test generation and testability analysis starting from a RTL VHDL description.

2) Definition of a methodology for the logic synthesis of self-checking control dominated circuits, starting from RTL-level synthesizable VHDL[55-57]. Testable macrocells have been written in VHDL, in particular BIST memories.

3) Development of a prototype testability analyzer and improver at RTL level, for different classes of circuits described in VHDL.

4) Methodology for hw/sw co-design of control dominated systems, based on VHDL for the hardware synthesis and for co-simulation [53, 54].

Prototype software for testability analysis and test pattern generation on a behavioral VHDL description, before high-level synthesis, is currently under development. A co-design environment for control dominated systems is also being written, including tools for self-checking synthesis and checker generation for Finite State Machines.

Most of the software developments are done jointly with Italtel, in the framework of Esprit projects PATRICIA and REQUEST, and are therefore not freely available outside. More information can be obtained from Donatella Sciuto (e-mail: sciuto@elet.polimi.it).

## 12. Università "La Sapienza", Rome, Italy [59]

The "Formal Methods for Systems Development" group headed by Rocco de Nicola gathers five researchers. Their area of interest is in the development of formal methods and verification tools. In cooperation with IEI-CNR at Pisa (Italy), they developed the system JACK (Just Another Concurrency Kit), which gathers a behavioral equivalence checker, a model checher, and a tool for the graphical presentation for semantic descriptions based on labelled transition systems. The tool is documented, distributed, and available by ftp from: rep1.iei.pi.cnr.it or http://rep1.iei.pi.cnr.it.

Within that framework, the activity on VHDL started in 1994. One researcher defined a clean semantics based on process algebras for a reasonable subset of VHDL, and established formal properties on language features [59]. The work has been interrupted in Roma due to the departure of the key team members during the fall. However, the work will be continued in Firenze, and will involve experiments using the VHDL semantics within the JACK system, in order to prove systems properties.

## 13. Politecnico di Torino, Italy [60-68]

The Dipartimento di Automatica e Informatica of Politecnico di Torino has been very active in CAD for VLSI circuits for over twenty years. The current CAD group in this Department gathers eight persons under the direction of Paolo Prinetto. Their topics of interest related to VHDL are Extensions for High-level Specifications, Formal verification from VHDL, Test and Reliabilty. Work on VHDL started in 1991, and the following results were achieved:

1) The definition of VOVHDL, an over-language to specify inter-process communications and synchronizations [60, 63]; the semantics of VOVHDL are defined in terms of a process algebra [15, 67]. VOVHDL is also simulatable, through the use of a translator from VOVHDL to VHDL.

2) The implementation of a translator from VOVHDL to the industrial Process Algebra verification tool ASA+ [64, 65], which is not publicly available since it was developed under contract from EDF and it requires the availability of COMPASS' VTIP and VERILOG's ASA+

3) The development of a home-made, BDD-based, Process-Algebra manipulation tool called SEVERO, which is a general tool based on the Circal algebra, and not a VHDL-specific tool [60-62, 68]. This sotware is available by ftp://ftp.polito.it/pub/people/panta . More information can be obtained by e-mail from: Fulvio Corno <corno@cclix1.polito.it> or Paolo Prinetto <prinetto@polito.it>.

Current research focuses on the following topics:

- Developing Design for Testability rules at the RT level, that take into account the effect of synthesis (e.g., how to direct your favourite synthesis tool to generate easily testable circuits)
- Analyzing testability of circuits at the system level (i.e., before scheduling and allocation), in order to evaluate the percentage of partial scan very early in the design process, and possibly propose modifications to the circuit
- Fault simulation of VHDL behavioral descriptions
- Dependability analysis through software fault injection via VHDL simulation.

## 14. Ecole Polytechnique Federale de Lausanne, Lausanne, Switzerland [69-70]

In the Integrated Systems Center of EPFL, large of 20 persons, a group around Alain Vachoux (e-mail: alain.vachoux@leg.de.epfl.ch) started working on VHDL in 1992. Their interest lies in the Analog extensions to VHDL, their primary objective being to contribute develop a new IEEE standard based on VHDL for the description and the simulation of analog and mixed analog-digital systems. They participate very actively in the IEEE 1076.1 Working Group, Alain Vachoux being vice-chair of this group. They also presented several talks and tutorials during European and US conferences and during industrial seminars to promote the VHDL-A development [69,70]. No software development is currently under way.

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